N-CHANNEL DOUBLE DIFFUSION MOS TRANSISTOR, AND SEMICONDUCTOR COMPOSITE DEVICE

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to an n-channel double diffusion MOS (Metal Oxide Semiconductor) transistor, and a semiconductor composite device including the same.

[0003] 2. Description of Related Art

[0004] US2010/0051946A1 discloses a BiCDMOS (Bipolar CMOS DMOS) device which is a semiconductor composite device including a bipolar element, a CMOS (Complementary MOS) transistor and a DMOS (Double Diffusion MOS) transistor provided on a common semiconductor substrate. An n-channel DMOS transistor generally has an n-type well provided on a p-type semiconductor substrate with the intervention of an n-type buried layer. In a surface portion of the n-type well, a p-type body layer and an n-type drift layer are provided in spaced relation, and a channel region is defined between the p-type body layer and the n-type drift layer. An n-type source layer is provided in the p-type body layer. In the n-type well, an n-type drain layer is provided in contact with the n-type drift layer. A gate electrode is provided in opposed relation to the channel region with the intervention of a gate insulation film.

[0005] With this arrangement, however, the n-type buried layer and the n-type drain layer are connected to the same node, so that a great capacitance present between the n-type buried layer and the p-type semiconductor substrate exerts a non-negligible influence on the through-rate. This makes it difficult to provide excellent switching characteristics. Since the p-type body layer is surrounded by the n-type well, a depletion layer cannot sufficiently laterally spread, making it impossible to reduce the ON resistance.

SUMMARY OF THE INVENTION

[0006] According to an embodiment of the present invention, there are provided an n-channel double diffusion MOS transistor having excellent switching characteristics, and a semiconductor composite device including the n-channel double diffusion MOS transistor.

[0007] The n-channel double diffusion MOS transistor according to the embodiment of the present invention includes: a p-type semiconductor substrate; a p-type epitaxial layer formed on the p-type semiconductor substrate through epitaxial growth; an n-type buried layer provided in a boundary between the p-type semiconductor substrate and the p-type epitaxial layer; a p-type body layer provided in a surface portion of the p-type epitaxial layer; an n-type source layer provided in the p-type body layer and defining a double diffusion structure together with the p-type body layer; an n-type drift layer provided in a surface portion of the p-type epitaxial layer in spaced relation from the p-type body layer to define a channel region between the n-type source layer and the n-type drift layer; an n-type drain layer provided in a surface portion of the p-type epitaxial layer in spaced relation from the channel region and in contact with the n-type drift layer; a p-type buried layer buried in the p-type epitaxial layer between the n-type drift layer and the n-type buried layer in contact with an upper surface of the n-type buried layer and having a lower impurity concentration than the n-type buried layer; a gate insulation film provided in a surface of the p-type epitaxial layer on the channel region; and a gate electrode provided in opposed relation to the channel region with the intervention of the gate insulation film.

[0008] Other elements, features, steps, characteristics and advantages of the present invention will become more apparent from the following detailed description of the preferred embodiments with reference to the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIG. **1** is a sectional view for explaining the construction of a semiconductor composite device according to an embodiment of the present invention.

[0010] FIGS. **2**A and **2**B are sectional views for explaining an exemplary structure of a CMOS area of the semiconductor composite device.

[0011] FIGS. **3**A to **3**C are sectional views for explaining an exemplary structure of a DMOS area of the semiconductor composite device.

[0012] FIGS. **4**A to **4**C are sectional views for explaining an exemplary structure of a bipolar area of the semiconductor composite device.

[0013] FIGS. **5**A to **5**C are sectional views for explaining an exemplary structure of a passive element area of the semiconductor composite device.

[0014] FIG. **6** is a diagram for explaining a process for fabricating the semiconductor composite device.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0015] According to an embodiment of the present invention, there is provided an n-channel double diffusion MOS transistor, which includes: a p-type semiconductor substrate; a p-type epitaxial layer formed on the p-type semiconductor substrate through epitaxial growth; an n-type buried layer provided in a boundary between the p-type semiconductor substrate and the p-type epitaxial layer; a p-type body layer provided in a surface portion of the p-type epitaxial layer; an n-type source layer provided in the p-type body layer and defining a double diffusion structure together with the p-type body layer; an n-type drift layer provided in a surface portion of the p-type epitaxial layer in spaced relation from the p-type body layer to define a channel region between the n-type source layer and the n-type drift layer; an n-type drain layer provided in a surface portion of the p-type epitaxial layer in spaced relation from the channel region and in contact with the n-type drift layer; a p-type buried layer buried in the p-type epitaxial layer between the n-type drift layer and the n-type buried layer in contact with an upper surface of the n-type buried layer and having a lower impurity concentration than the n-type buried layer; a gate insulation film provided in a surface of the p-type epitaxial layer on the channel region; and a gate electrode provided in opposed relation to the channel region with the intervention of the gate insulation film.

[0016] With this arrangement, the p-type body layer and the n-type drift layer are provided in the p-type epitaxial layer. The p-type epitaxial layer is isolated from the p-type semiconductor substrate by the n-type buried layer, and the p-type buried layer is provided between the n-type buried layer and the n-type drift layer in contact with the n-type buried layer. Therefore, the n-type drain layer contacting the n-type drift layer is electrically isolated from the n-type buried layer, so that a great capacitance present between the n-type buried